

APPENDIX

Please amend claim 1 as follows:

1 (Amended). A method comprising:

forming a buried line of a first [conductive] conductivity type in a bulk substrate, said buried line including a pair of more lightly doped regions [around] above and below a more heavily doped region;

creating a region of a second conductivity type opposite said first conductivity type [over said line] in said bulk substrate; and

forming a phase-change material over said region.

Please amend claim 11 as follows:

11 (Amended). A memory cell comprising:

a bulk substrate;

a phase-change material over said substrate;

a buried line of a first conductivity type formed in said substrate, said buried line including a [pair of] more lightly doped [regions around] region over a more heavily doped region and a more lightly doped region under said more heavily doped region; and

a region of a second conductivity type opposite said first conductivity type over said line and under said phase-change material.

Please amend claim 21 as follows:

21 (Amended). An electronic device comprising:

a system memory circuit including:

a [surface] bulk substrate;

a phase-change material over said [surface] substrate; [and]

a conductive line of a first conductivity type in said [surface having] substrate, said line including a more heavily doped region sandwiched between more lightly doped regions, said conductive line providing signals to said phase-change material; and

a region of a second conductivity type between said phase-change material and said conductive line; and

a processor coupled to said system memory circuit.